



SPECIFICATION FOR APPROVAL

MULTILAYER CERAMIC CHIP CAPACITOR

STANDARD TYPE MLCC



MULTILAYER CERAMIC CHIP CAPACITOR

***** STANDARD TYPE MLCC *****

FEATURES

- Nickel barrier end terminations to improve solderability.
- Multilayer block structure provides higher reliability.
- A wide range of capacitance values available in standard case sizes.

APPLICATIONS

- General electronic devices.

1. Product Identification

M	0603	N	101	J	050	T	A	X
1-1	1-2	1-3	1-4	1-5	1-6	1-7	1-8	1-9

1-1. **M** UWA Standard Type MLCC

1-2. **0603** Size

Code	EIA Code	Length * Width mm / (inch)
0201	0201	0.60 * 0.30 / (0.024 * 0.012)
0402	0402	1.00 * 0.50 / (0.04 * 0.02)
0603	0603	1.60 * 0.80 / (0.06 * 0.03)
0805	0805	2.00 * 1.25 / (0.08 * 0.05)
1206	1206	3.20 * 1.60 / (0.12 * 0.06)
1210	1210	3.20 * 2.50 / (0.12 * 0.10)
1812	1812	4.50 * 3.20 / (0.18 * 0.12)
2220	2220	5.70 * 5.00 / (0.22 * 0.20)

1-3. **N** Temperature Characteristic

Code	Temperature Characteristic	Capacitance Change	Operation Temperature Range
N	NPO	±30 ppm	-55 ~ +125
X	X7R	±15 %	-55 ~ +125
Y	Y5V	+22 ~ -82 %	-30 ~ +85
B	X5R	±15 %	-55 ~ +85
S	X6S	±22 %	-55 ~ +105
R	X5S	±22 %	-55 ~ +85
E	Y5U	+22 ~ -56 %	-30 ~ +85
Z	Z5U	+22 ~ -56 %	+10 ~ +85

1-4. **101** Capacitance

Code	Capacitance (pF)	Code	Capacitance (pF)
0R5	0.5	101	100
010	1	104	100,000 (100nF)
100	10	106	10,000,000 (10uF)



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1-5. **J** Capacitance Tolerance

Code	Tolerance	Nominal Capacitance
B	± 0.1 pF	10 pF
C	± 0.25 pF	
D	± 0.5 pF	
F	± 1 %	10 pF
G	± 2 %	
H	± 3 %	
J	± 5 %	
K	± 10 %	
M	± 20 %	
Z	- 20 % ~ + 80 %	

1-6. **050** Rated Voltage

Code	Rated Voltage	Code	Rated Voltage
006	6.3V	025	25V
010	10V	050	50V
016	16V		

1-7. **T** Quantity

(Unit : pcs)

Code	A	B	T	U	V	W	X	Y	Z			
7 "	15K	10K	4K	3K	2.5K	2K	1K	700	500			
Code	F	G	H	I	J	Code	L	M	N	R	P	Q
13 "	50K	15K	10K	4K	2K	Bulk	5K	10K	20K	50K	100K	200K

1-8. **A** Thickness

(Unit : mm)

Code	P	K	V	T	A	D	E	F
Thickness	0.3±0.03	0.45±0.05	0.5±0.05	0.7±0.1	0.8±0.1	0.85±0.1	1.0±0.1	1.15±0.1
Code	G	H	L	N	Y	M	U	
Thickness	1.25±0.2	1.5±0.2	1.6±0.2	1.9±0.2	2.0±0.2	2.5±0.2	3.2±0.3	

1-9. **N** Material Option

Code	Description Of The Code
N	Sn – Pb Plating (Sn 90% , Pb 10%)
X	Pb – Free Plating (Sn 100%)



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2. Standard Combination of Nominal Capacitance and Tolerance

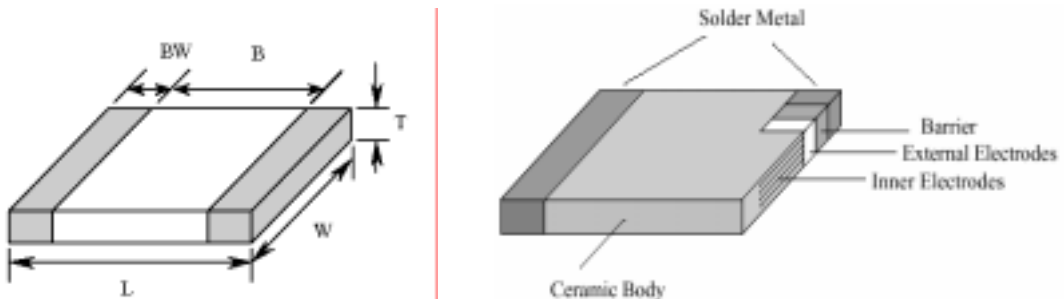
Class	Temperature Characteristic	Tolerance		Nominal Capacitance
Class I	NPO	Less Than 10pF	B(± 0.10 pF)	0.5,1,1.5,2,2.5,3
			C(± 0.25 pF)	0.5,1,1.5,2,2.5,3,3.5,4,4.5,5
			D(± 0.50 pF)	5,6,7,8,9,10
			F(± 1.00 pF)	6,7,8,9,10
		More Than 10pF	J($\pm 5\%$) B($\pm 10\%$)	E-24 series
Class II	X7R / X5R X5S / X6S	K($\pm 10\%$) , M($\pm 20\%$)		E-12 series
	Y5V	M($\pm 20\%$) , Z(-20 ~ +80%)		E- 6 series
	Y5U			
	Z5U			

Application Capacitance												
E-3	1.0				2.2				4.7			
E-6	1.0		1.5		2.2		3.3		4.7		6.8	
E-12	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2
E-24	1.0	1.2	1.5	1.8	2.2	2.7	3.3	3.9	4.7	5.6	6.8	8.2
	1.1	1.3	1.6	2.0	2.4	3.0	3.6	4.3	5.1	6.2	7.5	9.1

3. Dimension & Structure

(Unit : mm)

Code	L	W	T(max)	Bw
0201	0.60 \pm 0.03	0.30 \pm 0.03	0.33	0.15 \pm 0.05
0402	1.00 \pm 0.05	0.50 \pm 0.05	0.55	0.25 \pm 0.10
0603	1.60 \pm 0.10	0.80 \pm 0.10	0.95	0.35 \pm 0.15
0805	2.00 \pm 0.20	1.25 \pm 0.20	1.40	0.45 \pm 0.25
1206	3.20 \pm 0.30	1.60 \pm 0.20	1.80	0.50 \pm 0.20
1210	3.20 \pm 0.30	2.50 \pm 0.20	2.70	0.60 \pm 0.30
1812	4.50 \pm 0.40	3.20 \pm 0.30	3.30	0.80 \pm 0.40
2220	5.70 \pm 0.40	5.00 \pm 0.40	3.00	1.00 \pm 0.50





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4.Capacitance Range

Temperature Characteristic	Size Code	Rated Voltage	Capacitance Range (pF)							
			0R5 100	101	102	103	104	105	106	107
CLASS NPO	0201 (0603)	16	100							
		25	100							
	0402 (1005)	25	470							
		50	220							
	0603	50	1,000							
	0805	25	3,300					10,000		
		50	4,700							
1206	50	10,000								
CLASS X5R X6S X7R	0201 (0603)	6.3	1,000		10,000		10,000			
		10	1,000		6,800					
		16	100	1,000		4,700				
	0402 (1005)	6.3	100	100,000				220,000		220,000
		10	100,000							
		16	100,000							
		25	100	47,000						
		50	10,000							
	0603 (1608)	6.3	330,000			1,000,000		2,200,000		2,200,000
		10	100	680,000				1,000,000		1,000,000
		16	100	220,000		470,000				220,000
		25	100,000							
		50	100,000							
	0805 (2012)	6.3	2,200,000		4,700,000		10,000,000			10,000,000
		10	100	3,300,000			4,700,000			3,300,000
		16	100	1,000,000		3,300,000				1,000,000
		25	470,000							
		50	220,000							
	1206 (3216)	6.3	1,000		10,000,000		22,000,000			22,000,000
		10	1,000		10,000,000		22,000,000			22,000,000
		16	1,000		1,000,000		22,000,000			10,000,000
		25	1,000		1,000,000		10,000,000			4,700,000
		50	1,000		1,000,000					
	1210 (3225)	6.3	1,000,000		10,000,000		22,000,000			100,000,000
		10	220,000		4,700,000		22,000,000			22,000,000
		16	220,000		1,000,000		47,000,000			22,000,000
		25	220,000		1,000,000		10,000,000			10,000,000
50		220,000		1,000,000		2,200,000			4,700,000	
1812 (4532)	6.3	3,300,000		10,000,000		47,000,000			100,000,000	
	10	220,000		1,000,000		47,000,000			47,000,000	
	16	220,000		4,700,000		33,000,000			33,000,000	



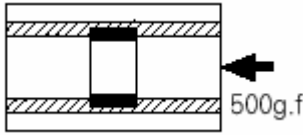
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Temperature Characteristic	Size Code	Rated Voltage	Capacitance Range (pF)								
			0R5 100	101	102	103	104	105	106	107	
CLASS X5R X7R	1812 (4532)	25					220,000	1,000,000	22,000,000	22,000,000	
		50					220,000	1,000,000	4,700,000	3,300,000	
	2220 (5755)	6.3						10,000,000	47,000,000	100,000,000	100,000,000
		10							33,000,000	100,000,000	100,000,000
		16						10,000,000	10,000,000	33,000,000	22,000,000
		25						10,000,000	4,700,000	22,000,000	10,000,000
		50						100,000		4,700,000	
CLASS Y5V	0402 (1005)	16			2,200					220,000	
		25			2,200					47,000	
		50			2,200					10,000	
	0603 (1608)	6.3							1,000,000		2,200,000
		10			2,200						1,000,000
		16			2,200						1,000,000
		25			2,200						330,000
		50			2,200						100,000
	0805 (2012)	6.3							4,700,000		10,000,000
		10							4,700,000		10,000,000
		16			10,000						4,700,000
		25			10,000						2,200,000
		50			10,000						1,000,000
	1206 (3216)	10							100,000		22,000,000
		16				10,000					10,000,000
		25				10,000					4,700,000
		50				10,000					1,000,000
	1210 (3225)	6.3							22,000,000		47,000,000
		10							10,000,000		22,000,000
		16			220,000						22,000,000
		25			220,000						10,000,000
		50			220,000						4,700,000
	1812 (4532)	6.3							47,000,000		100,000,000
		10							10,000,000		47,000,000
		16							10,000,000		22,000,000
		25							4,700,000		10,000,000
	2220 (5755)	10							100,000,000		100,000,000
		16							10,000,000		47,000,000
25								10,000,000		33,000,000	
50								4,700,000		10,000,000	



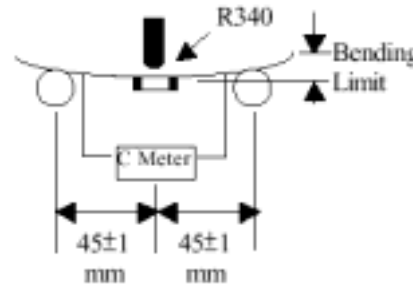
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5. Reliability And Test Conditions

No	Test Item	Specifications	Test Conditions										
1	Capacitance Class I NPO	Within The Specified Tolerance	Capacitance										
			Frequency										
			Signal Voltage										
	Capacitance Class II	Within The Specified Tolerance	C 1000 pF	1MHz ± 10%	1.0 ± 0.2Vrms								
			C > 1000 pF	1KHz ± 10%	1.0 ± 0.2Vrms								
Capacitance			Temp.Char.	Frequency	Rated Voltage								
C 22uF			X7R / X5R	1KHz ± 10%	1.0 ± 0.2Vrms								
	X6S / X5S	1KHz ± 10%	1.0 ± 0.2Vrms										
	Y5V	1KHz ± 10%	0.5 ± 0.2Vrms										
	C > 22uF	120Hz ± 20%	0.5 ± 0.1Vrms										
2	Q Class I NPO	C > 30 pF : Q 1000 C 30 pF : Q 400+20×C (C:Capacitance , pF)	Capacitance										
			Frequency										
			Signal Voltage										
	Tan (D.F.) Class II	Temp.Char.	HI-V	50V	25V	16V	10V	6.3V	Capacitance	Temp.Char.	Frequency	Signal Voltage	
		X7R / X5R	2.5%	2.5%	3.5%	3.5%	5%	5%	C 22uF	X7R / X5R	1KHz ± 10%	1.0 ± 0.2Vrms	
		X6S / X5S								X6S / X5S			
		Y5V	5%	5%	5%	9%	12.5%	16%		Y5V			1KHz ± 10%
		ALL								C > 22uF	120Hz ± 10%	0.5 ± 0.1Vrms	
		Special Parts											
		X7R / X5R / X6S / X5S						Y5V					
		Size	Rated Voltage	Capacitance		Tan		Size	Rated Voltage	Capacitance		Tan	
		0402	6.3V	C 0.22uF		10% max		0402	16V	C 220uF		12.5% max	
		0603		C 2.2uF				0603	25~50V	C 100nF		7% max	
		0805		C 4.7uF				0805	25~50V	C 330nF		7% max	
		1206		C 10uF				1206	25~50V	C 1uF		7% max	
1210	C 22uF			1210	25V			C 6.8uF		9% max			
1812	C 47uF			1812	10V			C 10uF		16% max			
2220	C 100uF			2220	-			-		-			
3	(I.R.) Insulation Resistance	Rated Voltage 25V 10,000 MΩ or 500MΩ ÷ uF		V _r 500V Applied Voltage:Rated Voltage									
		Rated Voltage 16V 10,000 MΩ or 100 MΩ ÷ uF	V _r 500V Applied Voltage:500V Applied Voltage:Rated Voltage Charge Time : 60 sec.										
4	Withstanding Voltage	No Dielectric Breakdown or Mechanical Breakdown	V _r < 100V Class I:300% of The Rated Voltage Class II:250% of The Rated Voltage V _r =100V 250% of The Rated Voltage 250V V _r < 500V 200% of The Rated Voltage 500V V _r < 1KV 150% of The Rated Voltage V _r 1KV 120% of The Rated Voltage For 1~5 sec. Is Applied Less Than 50mA Current										
5	Adhesive Strength Of Termination	No Indication Of Peeling Shall Occur On The Terminal Electrode.	A 500g.f Push or Pull Force Shall Be Applied For 10 ± 1 Seconds 										



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6	Resistance To Flexure Of Substrate	No Mechanical Damage Shall Occur.			Bending Shall Be Applied To The 1.0 mm With 1.0 mm / sec 	
		C-Meter	Temp. Char.	Cap. Change.		
			NPO	± 5 %		
			X7R / X5R X6S / X5S	± 12.5 %		
			Y5V	± 30 %		
			Y5U			
			Z5U			
			Chip Array Capacitor			
			NPO	± 1 %		
X7R	± 10 %					
Y5V						
7	Vibration	No Mechanical Damage Shall Be Occur			Vibrate The Capacitor With Amplitude Of 1.5mm P-P Changing The Frequencies From 10Hz to 55Hz And Back To 10Hz In About 1 min.	
		Capacitance	Temp. Char.			Cap. Change
			Class	NPO		Within±2.5%Or±0.25pF Whichever Is Larger
			Class	X7R / X5R X6S / X5S		Within ± 7.5 %
				Y5V/Y5U/Z5U		Within ± 20 %
		Q Class	C > 30 pF : Q 1000 C ≤ 30 pF : Q 400 + 20×C			
		Tan Class	To Satisfy The Specified Initial Value			
Insulation Resistance	To Satisfy The Specified Initial Value					
8	Capacitance Temperature Coefficient	Class I	Temp.Char	Temp. Range	Cap. Change	Class I: $\frac{C2-C1}{C1(T2-T1)} \times 100\%$ Class II : $\frac{C2-C1}{C1} \times 100\%$ T1:Standard Temperature (25°C) T2:Test Temperature C1:Capacitance At Standard Temperature (25°C) C2:Capacitance At Test Temperature (T2)
			NPO	-55°C~+125°C	± 30 ppm / °C	
		Class II	Temp.Char	Temp. Range	Cap. Change	
			X7R	-55°C~+125°C	± 15 %	
			X5R	-55°C~+85°C	± 15 %	
			X5S	-55°C~+85°C	± 22 %	
			X6S	-55°C~+105°C	± 22 %	
			Y5V	-30°C~+85°C	+ 22 % ~ - 82 %	
			Y5U	-30°C~+85°C	+ 22 % ~ - 56 %	
			Z5U	+10°C~+85°C	+ 22 % ~ - 56 %	



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9	Solderability	<p>More Than 75% of The Terminal Surface Is To Be Soldered Newly, So Metal Part Does Not Come Out Or Dissolve</p>	<p>Sn / Pb : Solder Temperature : 230 ± 5 °C Dip Time : 3 ± 1 sec. Solder : H63A Flux : RMA Type Preheat : At 80~120 °C For 10~30 sec. Pb Free : Solder Temperature : 250 ± 5 °C Dip Time : 3 ± 1 sec. Solder : H63A Flux : RMA Type Preheat : At 80~120 °C For 10~30 sec. Hand Soldering : Solder Temperature : Sn/Pb 230 ~ 280 °C . Pb Free 250 ~ 300°C Use a 20W Soldering Iron And The Soldering Iron Should Not Directly Touch Capacitor.</p>																																							
10	Resistance To Soldering Heat	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td colspan="3" style="text-align: center;">No Mechanical Damage Shall Be Occur</td> </tr> <tr> <td rowspan="4" style="width: 15%; text-align: center;">Capacitance</td> <td colspan="2" style="text-align: center;">Temp. Char.</td> <td style="text-align: center;">Cap. Change</td> </tr> <tr> <td style="text-align: center;">Class I</td> <td style="text-align: center;">NPO</td> <td style="text-align: center;">Within±2.5%Or±2.5pF Whichever Is Larger</td> </tr> <tr> <td rowspan="2" style="text-align: center;">Class II</td> <td style="text-align: center;">X7R / X5R X6S / X5S</td> <td style="text-align: center;">Within ± 10 %</td> </tr> <tr> <td style="text-align: center;">Y5V/Y5U/Z5U</td> <td style="text-align: center;">Within ± 20 %</td> </tr> <tr> <td style="text-align: center;">Q Class I</td> <td colspan="2">C > 30 pF : Q 1000 C 30 pF : Q 400+20×C</td> </tr> <tr> <td style="text-align: center;">Tanδ Class II</td> <td colspan="2">To Satisfy The Specified Initial Value</td> </tr> <tr> <td style="text-align: center;">Insulation Resistance</td> <td colspan="2">To Satisfy The Specified Initial Value</td> </tr> <tr> <td style="text-align: center;">Withstand Voltage</td> <td colspan="2">To Satisfy The Specified Initial Value</td> </tr> </table>	No Mechanical Damage Shall Be Occur			Capacitance	Temp. Char.		Cap. Change	Class I	NPO	Within±2.5%Or±2.5pF Whichever Is Larger	Class II	X7R / X5R X6S / X5S	Within ± 10 %	Y5V/Y5U/Z5U	Within ± 20 %	Q Class I	C > 30 pF : Q 1000 C 30 pF : Q 400+20×C		Tanδ Class II	To Satisfy The Specified Initial Value		Insulation Resistance	To Satisfy The Specified Initial Value		Withstand Voltage	To Satisfy The Specified Initial Value		<p>Class II capacitor shall be set for 48 ± 4 hours at room temperature after one hour heat treatment at 150+0/-10 °C before initial measure.</p> <p>Preheat : At 150±10°C For 60~120sec. Dip : Solder Temperature of 270±5°C Dip Time : 10±1sec. Solder : H63A Flux : Rosin</p> <p>Measure At Room Temp. After Cooling For: Class I : 24 ± 2 Hours Class II : 48 ± 4 Hours</p>												
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11	Temperature Cycle	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td colspan="3" style="text-align: center;">No Mechanical Damage Shall Be Occur</td> </tr> <tr> <td rowspan="4" style="width: 15%; text-align: center;">Capacitance</td> <td colspan="2" style="text-align: center;">Temp. Char.</td> <td style="text-align: center;">Cap. Change</td> </tr> <tr> <td style="text-align: center;">Class I</td> <td style="text-align: center;">NPO</td> <td style="text-align: center;">Within±2.5%Or±0.25 pF Whichever Is Larger</td> </tr> <tr> <td rowspan="2" style="text-align: center;">Class II</td> <td style="text-align: center;">X7R / X5R X6S / X5S</td> <td style="text-align: center;">Within ± 7.5 %</td> </tr> <tr> <td style="text-align: center;">Y5V/Y5U/Z5U</td> <td style="text-align: center;">Within ± 20 %</td> </tr> <tr> <td style="text-align: center;">Q Class I</td> <td colspan="2">C > 30 pF : Q 1000 C 30 pF : Q 400+20×C</td> </tr> <tr> <td style="text-align: center;">Tan δ Class II</td> <td colspan="2">To Satisfy The Specified Initial Value</td> </tr> <tr> <td style="text-align: center;">Insulation Resistance</td> <td colspan="2">To Satisfy The Specified Initial Value</td> </tr> </table>	No Mechanical Damage Shall Be Occur			Capacitance	Temp. Char.		Cap. Change	Class I	NPO	Within±2.5%Or±0.25 pF Whichever Is Larger	Class II	X7R / X5R X6S / X5S	Within ± 7.5 %	Y5V/Y5U/Z5U	Within ± 20 %	Q Class I	C > 30 pF : Q 1000 C 30 pF : Q 400+20×C		Tan δ Class II	To Satisfy The Specified Initial Value		Insulation Resistance	To Satisfy The Specified Initial Value		<p>Class II capacitor shall be set for 48 ± 4 hours at room temperature after one hour heat treatment at 150+0/-10 before initial measure.</p> <p>Capacitor Shall Be Subjected To Five Cycles Of The Temperature Cycle As Following:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 10%;">Step</th> <th style="width: 50%;">Temp (°C)</th> <th style="width: 40%;">Time(min)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">1</td> <td style="text-align: center;">Min Rated Temp +0/-3</td> <td style="text-align: center;">30</td> </tr> <tr> <td style="text-align: center;">2</td> <td style="text-align: center;">25</td> <td style="text-align: center;">3</td> </tr> <tr> <td style="text-align: center;">3</td> <td style="text-align: center;">Max Rated Temp +0/-3</td> <td style="text-align: center;">30</td> </tr> <tr> <td style="text-align: center;">4</td> <td style="text-align: center;">25</td> <td style="text-align: center;">3</td> </tr> </tbody> </table> <p>Measure At Room Temp. After Cooling For: Class I : 24 ± 2 Hours Class II : 48 ± 4 Hours</p>	Step	Temp (°C)	Time(min)	1	Min Rated Temp +0/-3	30	2	25	3	3	Max Rated Temp +0/-3	30	4	25	3
No Mechanical Damage Shall Be Occur																																										
Capacitance	Temp. Char.		Cap. Change																																							
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	Class II	X7R / X5R X6S / X5S	Within ± 7.5 %																																							
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Step	Temp (°C)	Time(min)																																								
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2	25	3																																								
3	Max Rated Temp +0/-3	30																																								
4	25	3																																								



MULTILAYER CERAMIC CHIP CAPACITOR

12	High Temperature	No Mechanical Damage Shall Be Occur							Class capacitors applied DC voltage is applied for one hour at maximum operation temperature ± 3 then shall be set for 48 ± 4 hours at room temperature and the initial measurement shall be conducted. Applied Voltage : V_r 200V : 200% Of Rated Voltage V_r 250V : 120% Of Rated Voltage Temperature : Maximum Operation Temperature Test Time : 1000 + 48/ - 0 Hour Current Applied : 50mA Max. Measurement Room Temperature After Cooling For : Class : 24 \pm 2 Hour Class : 48 \pm 4 Hour		
		Capacitance	Temp. Char.			Cap. Change					
			Class	NPO			Within $\pm 3.0\%$ Or $\pm 0.3pF$ Whichever Is Larger				
			Class	X7R / X5R X6S / X5S			Within $\pm 15\%$				
		Y5V/Y5U/Z5U			Within $\pm 30 \sim 40\%$						
Q Class	$C > 30pF$: Q 350 $10 pF < C \leq 30 pF$: Q $275 + 2.5 \times C$ $C \leq 10 pF$: Q $200 + 10 \times C$										
Tan Class	Temp. Char.	HI-V	50V	25V	16V	10V	6.3V				
	X7R / X5R X6S / X5S	5%	5%	7%	7%	10%	12.5%				
	Y5V	7.5%	7.5%	10.5%	12.5%	15%	20%				
	Y5U / Z5U	5%	6%	10.5%	10.5%	-	-				

13	Humidity	No Mechanical Damage Shall Be Occur							Class II capacitor shall be set for 48 ± 4 hours at room temperature after one hour heat treatment at 150 ± 10 °C before initial measure. Temperature : 40 ± 2 °C Relative Humidity : 90 ~ 95 % RH Test Time : 500+12/-0 Hour Current Applied : 50mA Max. Measurement Room Temperature After Cooling For : Class I : 24 \pm 2 Hours Class II : 48 \pm 4 Hours		
		Capacitance	Temp. Char.			Cap. Change					
			Class I	(NPO)			Within $\pm 5\%$ Or $\pm 0.5pF$ Whichever Is Larger				
			Class II	X7R / X5R			Within $\pm 15\%$				
		Y5V/Y5U/Z5U			Within $\pm 30\%$						
Q Class I	$C > 30 pF$: Q 350 $10 pF < C \leq 30 pF$: Q $275 + 2.5 \times C$ $C \leq 10 pF$: Q $200 + 10 \times C$										
Tan δ Class II	Temp. Char.	HI-V	50V	25V	16V	10V	6.3V				
	X7R / X5R X6S / X5S	2.5%	5%	7%	7%	10%	12.5%				
	Y5V	7.5%	7.5%	10.5%	12.5%	15%	20%				
	Y5U / Z5U	5%	6%	6%	6%	-	-				
Insulation Resistance	Minimum Insulation Resistance : 1000 M Ω or 50 M Ω \div μF product whichever is smaller										



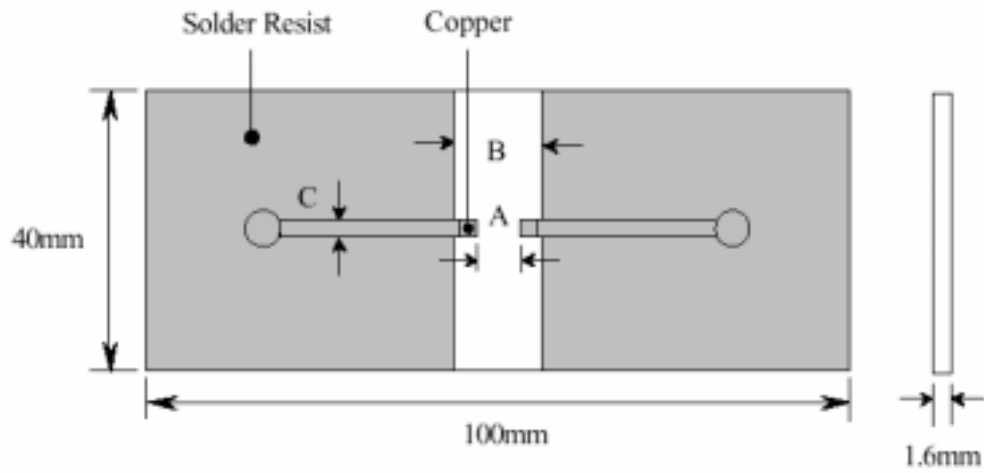
MULTILAYER CERAMIC CHIP CAPACITOR

14	Humidity Load	No Mechanical Damage Shall Be Occur						Class capacitors applied DC voltage of the rated voltage is applied for one hour at maximum operation temperature ± 3 then shall be set for 48 ± 4 hours at room temperature and the initial measurement shall be conducted Applied Voltage : Rated Voltage Temperature : 40 ± 2 Relative Humidity : 90 ~ 95% RH Test Time : $500 + 12/ - 0$ Hour Current Applied : 50mA Max. Measurement Room Temperature After Cooling For : Class : 24 ± 2 Hour Class : 48 ± 4 Hour s			
		Capacitance	Temp. Char.			Cap. Change					
			Class	NPO			Within $\pm 7.5\%$ Or $\pm 0.75\text{pF}$ Whichever Is Larger				
			Class	X7R / X5R X6S / X5S			Within $\pm 12.5\%$				
		Y5V/Y5U/Z5U			Within $\pm 30 \sim 40\%$						
Q Class	C > 30 pF : Q 350 10 pF < C 30 pF : Q $275 + 2.5 \times C$ C 10 pF : Q $200 + 10 \times C$						Chip Array Capaitor C > 30 pF : Q 200 C 30 pF : Q $200 + 10 / 3 \times C$				
	Tan Class	Temp. Char.	HI-V	50V	25V	16V		10V	6.3V		
X7R/X5R X6S / X5S		2.5%	5%	7%	7%	10%	12.5%				
Y5V		7.5%	7.5%	10.5%	12.5%	15%	20%				
Y5U / Z5U		5%	6%	6%	6%	-	-				
Insulation Resistance	Minimum Insulation Resistance: $500M$ or $25M \div \mu F$ Product Whichever Is Smaller.										
15	Soldering Reference List	Size	Char. Temp	Capacitance				Condition			
				Reflow		Flow					
		0201	All	All					x		
		0402	All	All					x		
		0603	NPO / X5R / X7R X6S / X5S	All							
				Y5V		C < 1uF					
				C 1uF			x				
		0805	NPO / X5R / X7R X6S / X5S	All							
				Y5V		C < 4.7uF					
				C 4.7uF			x				
		1206	NPO / X5R / X7R X6S / X5S	All							
				Y5V		C < 10uF					
		C 10uF			x						
1210 1808 1812 2220	All	All					x				



MULTILAYER CERAMIC CHIP CAPACITOR

6. P.C. Board for Bending Strength Test



Unit : mm

Code	A	B	C
0201	0.2	1.0	0.3
0402	0.4	1.4	0.5
0603	1.0	3.0	1.0
0805	1.2	4.0	1.6
1206	2.2	5.0	2.0
1210	2.2	5.0	2.9
1808	3.5	7.0	2.5
1812	3.5	7.0	3.7
2220	4.5	8.0	5.6

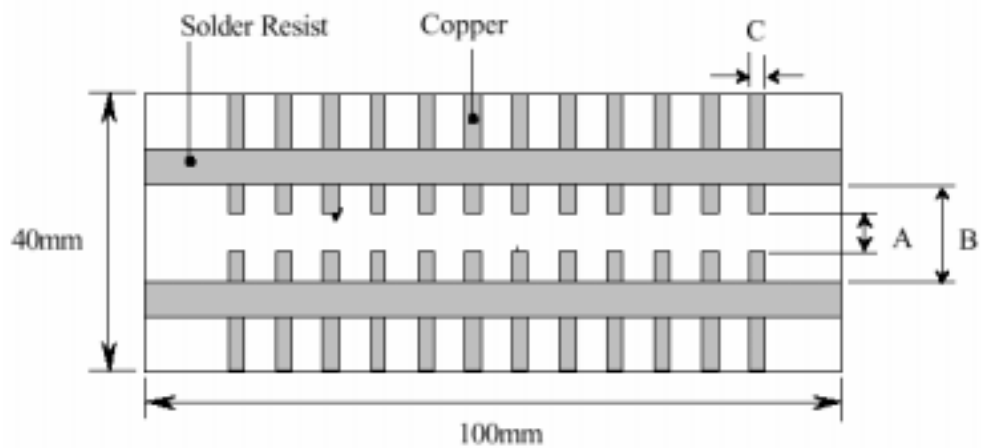
7. Test Substrate

Material: Glass Epoxy Substrate

■ : Copper (Thickness : 0.035mm)

■ : Solder Resist

Test Substrate



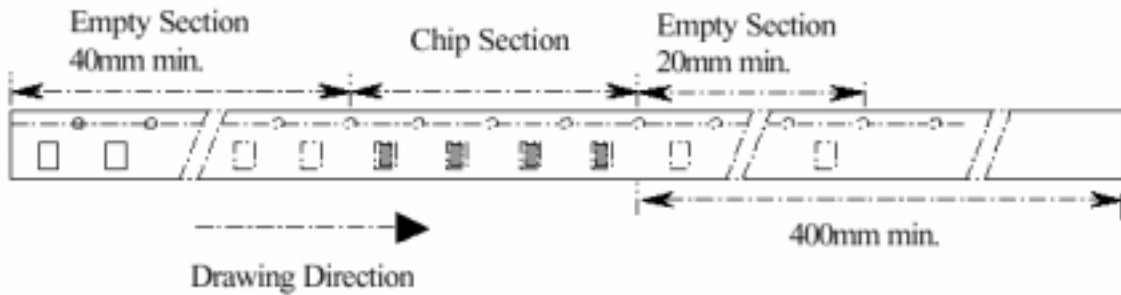


MULTILAYER CERAMIC CHIP CAPACITOR

Unit: mm

Code	A	B	C
0201	0.2	1.0	0.3
0402	0.4	1.4	0.5
0603	1.0	3.0	1.0
0805	1.2	4.0	1.6
1206	2.2	5.0	2.0
1210	2.2	5.0	2.9
1808	3.5	7.0	2.5
1812	3.5	7.0	3.7
2220	4.5	8.0	5.6

8. Packaging



8-3. Material And Quantity

Size	Thickness (mm)	7 " Reel		13 " Reel
		Paper Tape	Plastic Tape	Paper / Plastic
0201	T 0.33	10K pcs / Reel	-	-
0402	T 0.55	10K pcs / Reel	-	50K pcs / Reel
0603	T 0.95	4K pcs / Reel	-	10K / 15K pcs / Reel
0805	T 0.95	4K pcs / Reel	-	10K / 15K pcs / Reel
	0.95 < T 1.45	-	3K / 2K pcs / Reel	-
1206	T 0.95	4K pcs / Reel	-	10K pcs / Reel
	0.95 < T 1.45	-	3K / 2K pcs / Reel	-
	T > 1.45	-	2K pcs / Reel	-
1210	T 1.45	-	3K pcs / Reel	10K pcs / Reel
	T > 1.45	-	2K pcs / Reel	4K pcs / Reel
1808	T 1.45	-	3K pcs / Reel	10K pcs / Reel
	T > 1.45	-	2K pcs / Reel	4K pcs / Reel
1812	T 2.22	-	1K pcs / Reel	4K pcs / Reel
	T > 2.22	-	500 pcs / Reel	4K pcs / Reel
2220	T 2.22	-	1K pcs / Reel	2K pcs / Reel
	T > 2.22	-	500 pcs / Reel	2K pcs / Reel

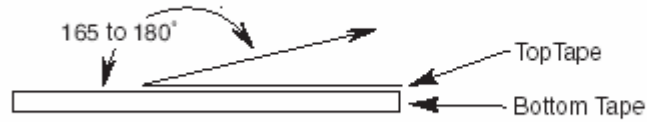


MULTILAYER CERAMIC CHIP CAPACITOR

8-1. Cover Tape Reel Off Force

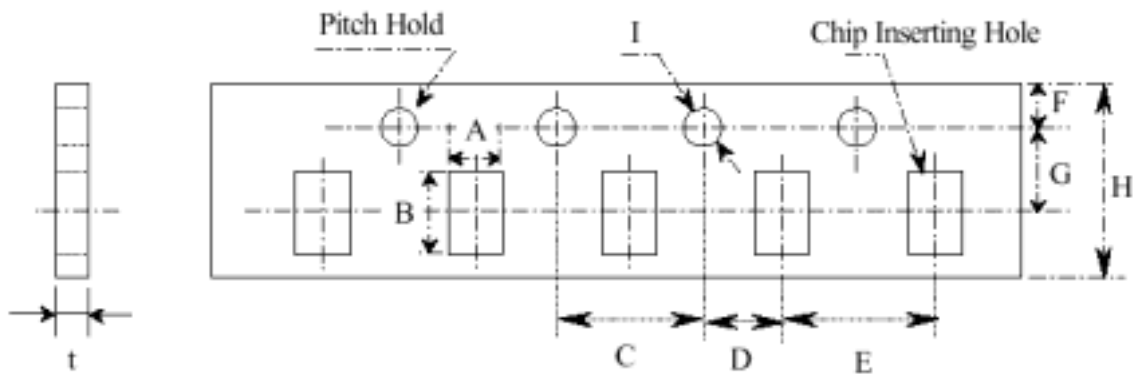
Peel-Off Force : 5 g . f Peel-Off Force 70 g . f

Cover Tape reel Off Force



The for peel off cover tape is 5 to 70 grams in the arrow direction.

8-2. Paper Tape



Unit: mm

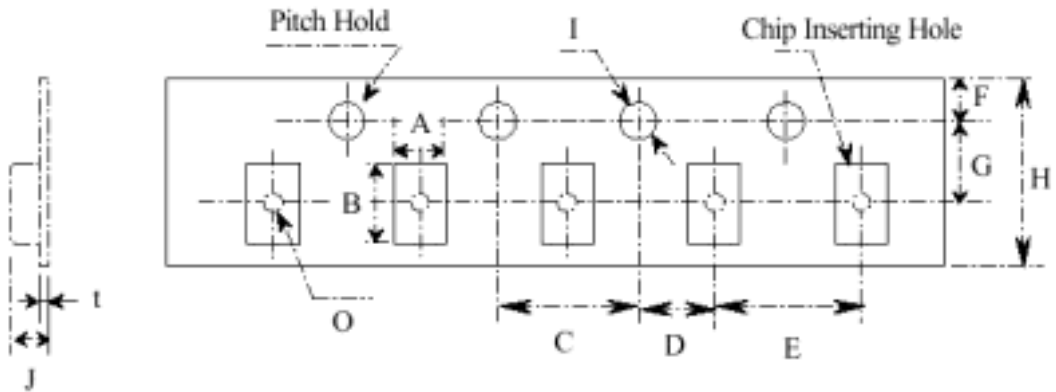
Code	A	B	C	D	E
0201	0.37±0.03	0.67±0.03	2.0±0.1	1.0±0.05	2.0±0.1
0402	0.61±0.10	1.2±0.1			
0603	1.10±0.20	1.9±0.2	4.0±0.1	2.0±0.05	4.0±0.1
0805	1.50±0.20	2.3±0.2			
1206	1.90±0.20	3.5±0.2			
1210	2.90±0.20	3.6±0.2			

Code	F	G	H	I	J
0201	1.75±0.1	3.5±0.05	8.0±0.3	1.5 + 0.1/ - 0	1.1max
0402					
0603					
0805					
1206					
1210					



MULTILAYER CERAMIC CHIP CAPACITOR

8-3. Plastic Tape



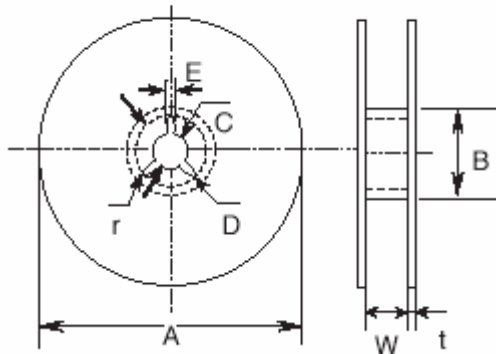
Unit: mm

Code	A	B	C	D	E	F
0805	1.5±0.2	2.3±0.2	4.0±0.1	2.0±0.05	4.0±0.1	1.75±0.1
1206	1.9±0.2	3.5±0.2				
1210	2.9±0.2	3.6±0.2				
1808	2.5±0.2	4.9±0.2			8.0±0.1	
1812	3.6±0.2	4.9±0.2				
2220	5.4±0.2	6.1±0.2				

Code	G	H	I	J	t	O
0805	3.5±0.05	8.0±0.3	1.5 + 0.1/ - 0	2.7 max.	0.3 max.	1.5 min.
1206				3.3 max.		
1210						
1808	5.5±0.05	12.0 + 3/ - 0		3.3 max.		
1812						
2220						

8-4. Reel Dimensions

Material: Paper, Plastic



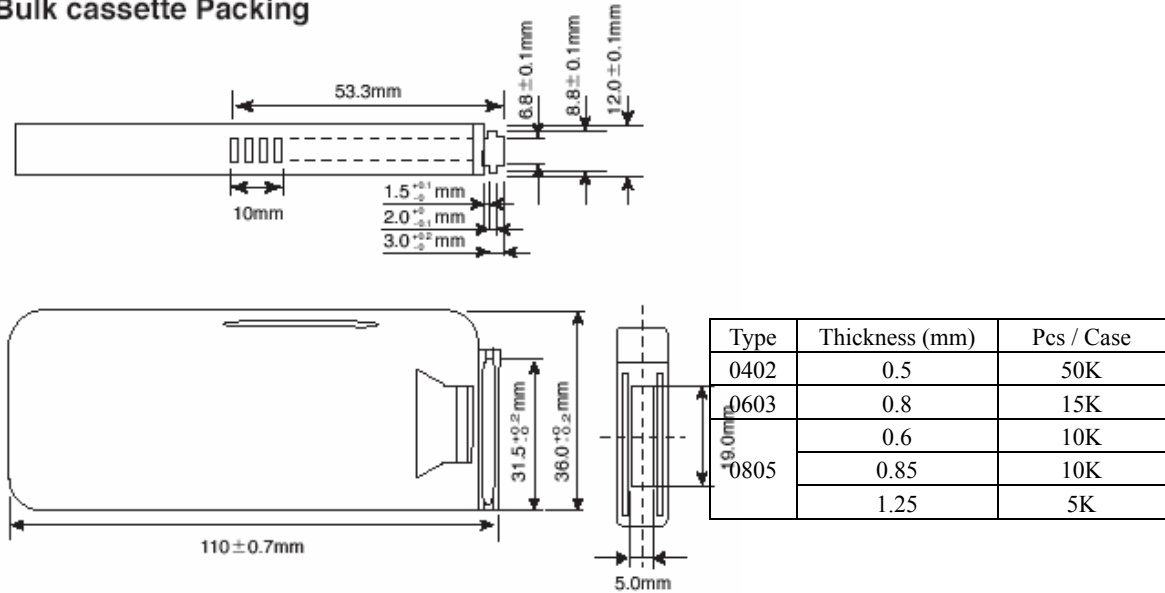
Tape Size	7 " Reel		13 " Reel	
	8mm	12mm	8mm	12mm
A	178±2		330±2	
B	50±2		60±2	
C	13±0.5		13±0.5	
D	21±1		21±1	
E	2±0.5		2±0.5	
W	10±1.5	14±2	10±1.5	14±2
T	1.5±0.5		2±1	
r	1.0		1.0	



MULTILAYER CERAMIC CHIP CAPACITOR

8-5. Bulk Cassette Quantity

Bulk cassette Packing



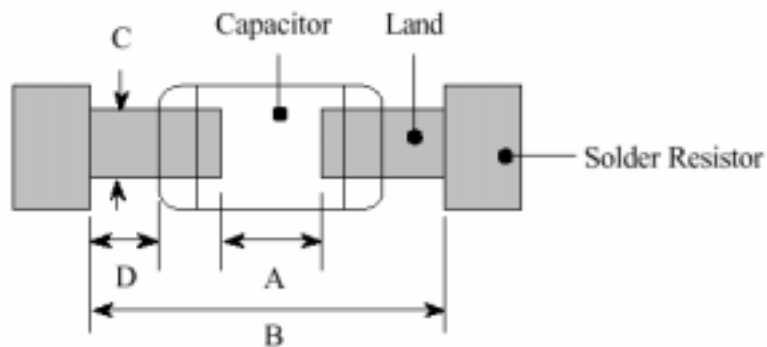
9. Precaution Of Usage

9-1. Storage

Store the capacitors where the temperature and relative humidity don't exceed 40°C and 70°RH.

We recommend you use capacitors within 6 months from the manufactured date. In case of packaging, don't the last wrapped, polyethylene bag, till just before using. If it is opened, seal it as soon as possible or keep it in a desiccant with a desiccation agent.

9-2. Size and recommend land dimensions.





MULTILAYER CERAMIC CHIP CAPACITOR

Unit : mm

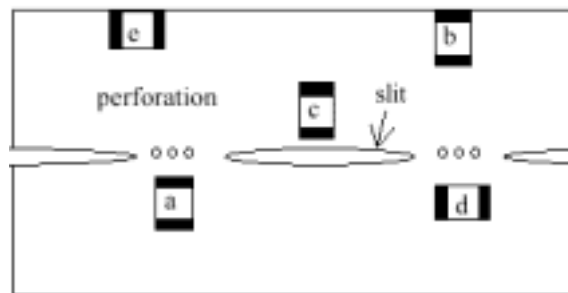
Code	Chip Capacitor		Land			
	L	W	A	B	C	D
0201	0.60	0.30	0.2~0.3	0.9~1.1	0.2~0.3	0.1~0.3
0402	1.00	0.05	0.3~0.5	1.3~1.5	0.3~0.5	0.1~0.3
0603	1.60	0.80	0.6~0.8	1.9~2.1	0.6~0.8	0.2~0.5
0805	2.00	1.25	0.8~1.2	2.4~3.2	0.9~1.2	0.2~0.6
1206	3.20	1.60	1.8~2.5	3.8~4.8	1.2~1.6	0.3~0.8
1210	3.20	2.5	1.9~2.6	3.9~4.9	1.9~2.5	0.3~0.8
1808	4.50	2.00	2.4~3.4	5.4~6.0	1.7~2.0	0.5~1.3
1812	4.50	3.20	2.5~3.5	5.5~6.1	2.3~3.2	0.5~1.3
2220	5.70	5.00	2.7~4.2	6.7~8.3	3.5~5.0	0.5~1.3

9-3..Mechanical strength varies according to location of chip capacitors the P.C. board.

Design layout of components on the PC board to minimize the stress imposed on the wrap or flexure of the board.

Component layout close to board break

Susceptibility to stress is in the order of : $a > b > c$ $d > e$



9-4.Layout Recommendation

Example	Use of Common Solder Land	Solder With Chassis	Use of Common Solder Land With Other SMD
Need to Avoid			
Recommendation			

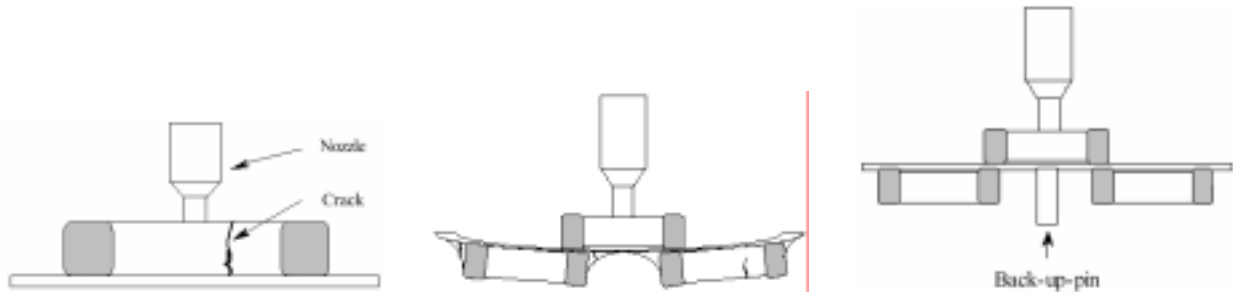


MULTILAYER CERAMIC CHIP CAPACITOR

9-5. Mounting

Crack is caused by impact load due to suction nozzle at the mounted.

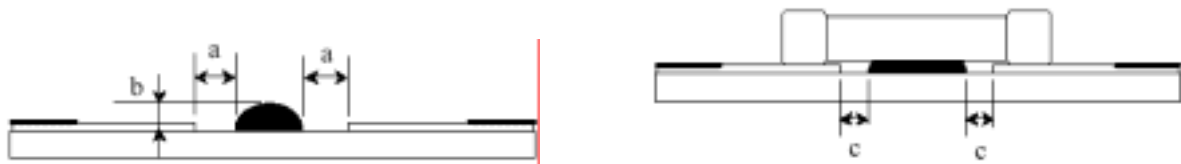
In mounting an element to board, If the low dead point is too low, excessive stress is applied to element. This will cause cracking. In this case, it is required to shift the low dead point of a suction nozzle to the upper surface of board so that warping of board is eliminated. Nozzle pressure is adjusted to 1N to 3N (static load) during mounting.



To Fix Board With Support Pin (OK)

If board is warped during mounting, crack or peeling of soldering will be caused. To avoid this, it is required to fix the board with back up pins or the like to avoid warping. Also, similar precautions are required when inserting a part with lead.

9-6. Amount of Adhesive



Example : 0805 & 1206 Size MLCC	
A	0.2mm (min)
B	70 ~ 100 μ M
C	Do Not Touch The Solder Land

9-7. Soldering

9-7-1. Avoiding Thermal Shock

(a) preheat Condition

Carefully perform pre-heating so that the temperature difference (T) between the solder and component surface should be in the follow range.

Soldering Method	3.2x1.6mm max.	3.2x1.6mm min.
Reflow method	T 190°C	T 190°C
Immersion method	T 150°C	T 100°C

(b) Colling Condition

Natural colling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (T) must be less than 100°C

9-7-2. Recommend Soldering Profile By various Methods

Infrared reflow soldering standard condition Iron/immersion soldering standard condition

9-7-3. Amount of Solder

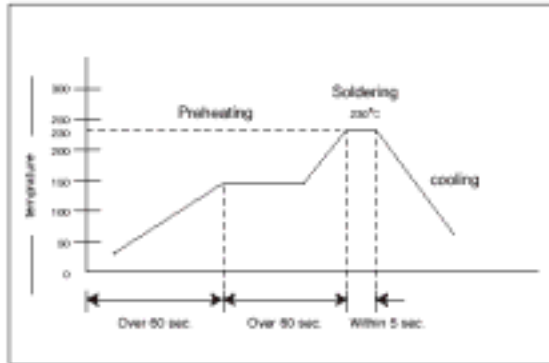
Excessive solder will induce higher tensile force in chip capacitor when temperature change and it may result in chip cracking. In Sufficient solder may detach the capacitor from the P.C. board.



MULTILAYER CERAMIC CHIP CAPACITOR

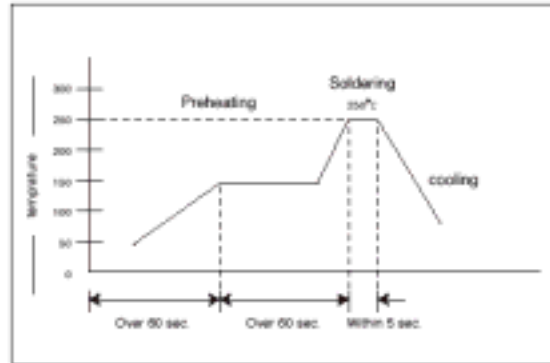
Sn/Pb Plating

Reflow

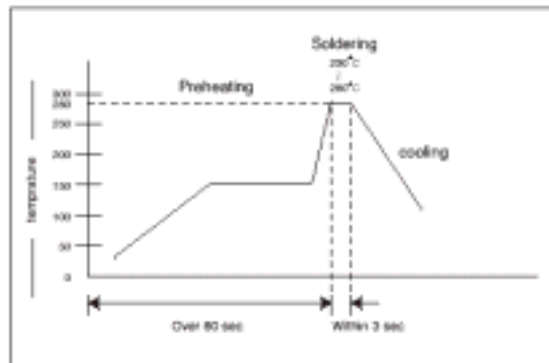


Pb-Free (Sn 100%) Plating

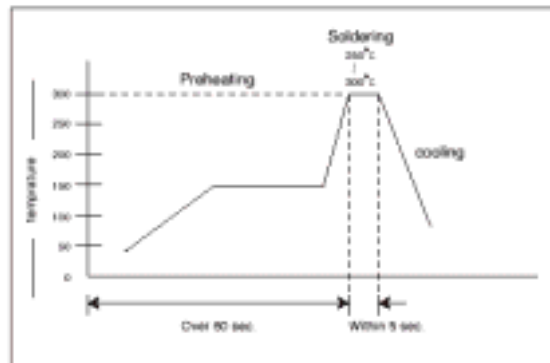
Reflow



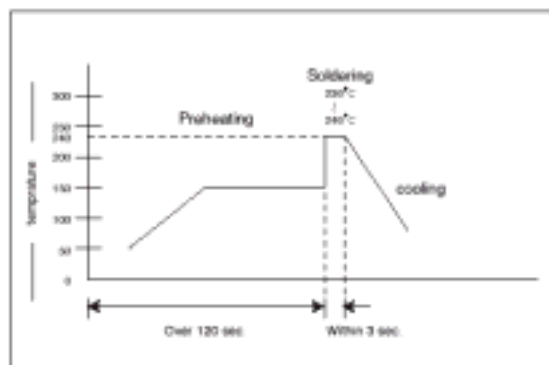
Solder Iron



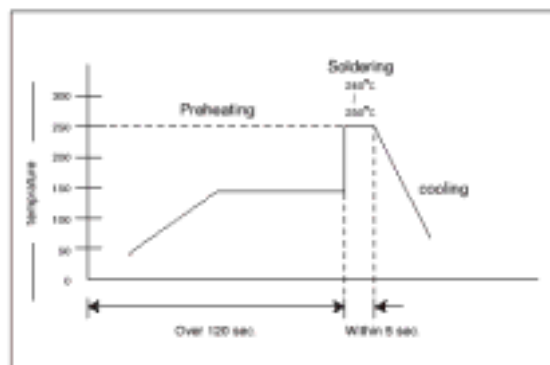
Solder Iron



Flow

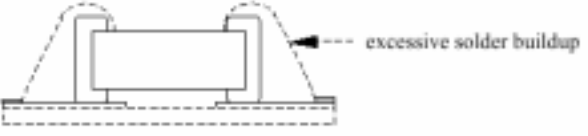





Flow



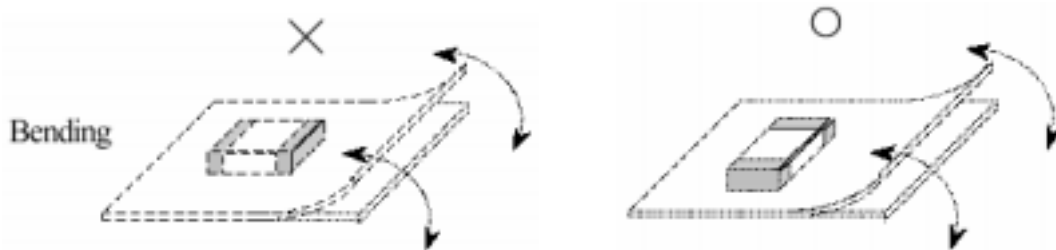


MULTILAYER CERAMIC CHIP CAPACITOR

Excessive Solder	
Adequate	
Insufficient Solder	
Solder buildup by Reflow method	

10. Caution : Handling after chip mounted

10-1. Please pay attention put the component lateral to the direction in which stress acts.



10-2. Crack Will be caused if board is warped due to excessive load by check pin.

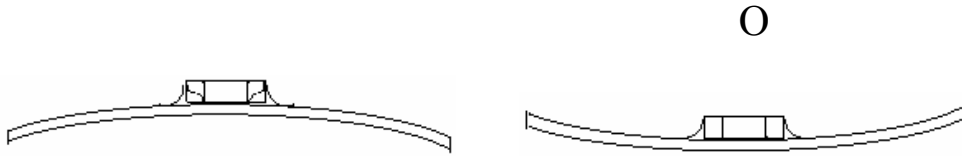




MULTILAYER CERAMIC CHIP CAPACITOR

10-3. Mechanical stress due to warping and torsion by dividing.

- (a) Crack occurrence ratio will be increased by manual separation.
- (b) Crack occurrence ratio will be increased by tensile force, rather than compressive force.



10-4. Handling to Loose Chip Capacitor

- (a) IF dropped the chip capacitor may crack.
- (b) Piling the P.C. board after mounting for storage or handling, the corner of the P.C. board may hit the chip capacitor of another of board to cause crack.

